SYSTEM AND METHOD FOR REDUCING CLOCK SKEW

ABSTRACT

In one embodiment, a method for balancing clock signals in a clock tree includes, at a register, receiving a divided input clock signal and a non-divided input clock signal and generating a first output clock signal based on the received divided input clock signal and the received non-divided input clock signal, the first output signal being associated with a first delay. The method further includes, at a delay line, receiving the non-divided input signal, delaying the non-divided input signal for a time substantially equivalent to the first delay, and generating a second output clock signal associated with a second delay substantially equal to the first delay. The method further includes: (1) receiving at a multiplexer the first output signal, the second output signal, and a select control signal indicating which of the first output signal or the second output signal to select; (2) selecting at the multiplexer either the received first output signal or the second output signal based on the select control signal; and (3) generating the selected first output signal or second output signal as a substantially balanced third output signal.